DECLARATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: Takaaki Shiota, Yoshinobu Nakada

Filling Date: November 13, 2003

Application No.: 10/706,266

Group Art Unit: 1722 Examiner: ROBERT M. KUNEMUND

Title: SILICON WAFER AND MANUFACTURING METHOD THEREOF

DECLARATION PURSUANT TO 37 C.F.R. 1.132

Commissioner for Patents

Washington, D.C. 20231

Sir:

I, Takaaki Shiota, residing at Saga Prefecture, Japan, declare and state that

1. I graduated from Kyoto University, Department of Science, in March 1986. Since April 1986, I have been employed by SUMCO CORPORATION, and have been engaged in research and development.

2. I am one of the inventors of the invention as claimed in the above-referenced application, and accordingly, I am familiar with the specification and claims of that application.

3. I am aware of the Office Action of September 29, 2005, issued on the

above-referenced application, in which the present invention was rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application No. 6,849,901 (Falster).

4. As is described in this Declaration, I conducted experiments for the purpose of demonstrating that remarkable effects can be obtained by subjecting a silicon wafer to vacancy heat treating so as to nitride the surface thereof in claim 6 of the present invention.

1. Formation of Vacancies (vacancy heat treating)

1-1. Methods for Preparing Samples

Silicon wafers having a thickness of 725 μm and a diameter of 200 mm were cut from an ingot, and subjected to the following RTA treatments (heat treatment involving rapid heating and cooling).

Sample 1

Using the heat treatment furnace shown in FIG. 1 of the specification, the silicon wafer was mounted on a susceptor 1, and then pure Ar was supplied to the surface of the silicon wafer from a supply port 2a, displacing the atmosphere in the heat treatment furnace, and thus purging it of oxygen. With oxygen completely removed from the furnace, the temperature was raised to 800°C while supplying pure Ar.

NH_3 was then introduced to the heat treatment furnace, and the temperature was raised from 800°C to a heat treatment temperature of 1150°C at a rate of temperature rise of 50°C/min. while supplying a mixture of Ar and NH_3 as the atmosphere. The heat treatment temperature of 1150°C was maintained for 10 seconds, after which it was cooled to 800°C at a rate of temperature reduction of 70°C/min.

Then, with the heat treatment temperature maintained at 800°C, pure Ar was supplied as the atmosphere at an increased flow rate until the NH_3 was discharged completely. Then, after the NH_3 had been discharged completely, cooling proceeded in the pure Ar atmosphere.

Sample 2

Sample 2 was prepared in a same manner as for Sample 1, except that N_2 was used instead of NH_3 and the heat treatment temperature was 1250°C.

Sample 3 (same as first embodiment of Falster)

Sample 3 was prepared in a same manner as for Sample 2, except that prior to the RTA treatment, the silicon wafer was heat-treated in an N_2 atmosphere containing oxygen of 1% at 1000°C for 10 min. and the heat treatment time was 35 seconds instead of 10 seconds.

1-2. Method for measuring vacancy concentration

Pt was dispersed by Frank-Turnbull dispersion at a constant condition, and the vacancy concentration profile in a depth direction of the silicon wafer was measured by deep level transient spectroscopy (DLTS).

1-3. Results and Discussion

The measurements are shown in REFERENCE FIG. 1.

The vacancy concentration profiles of samples 1 and 2 have the same characteristics. In Sample 1, a high concentration of vacancies are formed in the interior near the surface (at or in the vicinity of a depth of 50 μm). In the vacancy concentration profile, starting at a depth of about 50 μm or more, the vacancy concentration decreases as the depth increases. In Sample 2, a high concentration of vacancies are formed in the interior near the surface (at or in the vicinity of a depth of about 65 μm). In the vacancy concentration profile, starting at a depth of about 65 μm or more, the vacancy

concentration decreases as the depth increases.

In contrast, in the vacancy concentration profile of Sample 3, the vacancy concentration near the surface is very low. The vacancy concentration increases as the depth increases, that is, the vacancy concentration near the surface is lower than that in the mid-section of the silicon wafer.

The reasons why the differences between Sample 1 (Sample 2) and Sample 3 occurred can be explained as follows.

REFERENCE FIG. 2 (a) shows an imaginary view of vacancy-injection by surface nitriding. When the surface of the silicon wafer is nitrided (Samples 1 and 2), silicon atoms are bonded with nitrogen atoms in the surface, and vacancies are formed in the surface. Then, vacancies are dispersed in a bulk portion. Therefore, in Samples 1 and 2, a high concentration of vacancies are formed in the interior near the surface, and the vacancy concentration near the surface is higher than that in the mid-section of the wafer.

REFERENCE FIG. 2 (b) shows an imaginary view of vacancy-formation by creation of Frenkel pairs. When the silicon wafer having an oxide layer in the surface thereof is heated in an inert gas (Sample 3), pairs of vacancies and interstitial silicons are created (creations of Frenkel pairs). Interstitial silicon diffuses quickly, and only the vacancies remain and are frozen after rapid cooling, so that vacancies are formed. Since the Frenkel pairs are created in the interior of the silicon wafer, in Sample 3, the vacancy concentration near the surface is lower than that in the mid-section of the silicon wafer.

Next, the differences between Sample 1 and Sample 2 are explained as follows. In both Sample 1 and Sample 2, maximum vacancy concentration can be obtained in the interior near the surface (at depths of about 50 μm and 65 μm, respectively), and the values of the maximum vacancy concentrations are almost the same (1.3×10^{13} cm^{-3} and 1.45×10^{13} cm^{-3}, respectively). However, the heating temperature for Sample 1 is about 100°C lower than that for Sample 2. Therefore, it can be assumed that in the case in which an

atmosphere containing NH_3 is used (Sample 1), the heat treatment temperature can be lowered by about 100°C compared to the case in which an atmosphere of N_2 is used (Sample 2), for the purpose of forming the same concentration of vacancies in the interior near the surface.

Therefore, in the case in which the silicon wafer is subjected to vacancy heat treating in an atmosphere containing NH_3, a high concentration of vacancies are formed in the interior near the surface at low temperature.

In comparison with the case in which the silicon wafer is heated at high temperature in the atmosphere of N_2, in the vacancy concentration profile in the case in which the silicon wafer is heated at low temperature in the atmosphere of NH_3, vacancy concentration decreases more rapidly as the depth from the surface increases. In particular, vacancy concentration in the mid-section of the silicon wafer is low.

2. Observation of slip dislocation

2-1. Methods for Preparing samples

Samples were prepared in the same manner as for Sample 1 of "1. Formation of Vacancies", except that the heat treatment temperature was 1150, 1170, 1175, 1200 or 1220°C, and the silicon wafer was supported at three positions (Nos. 1 to 3 as shown in FIG. 4) of the rear surface while the heat treating.

2-2. Method for Measuring Depth of Region Free of Slip Dislocations

As shown in FIG. 3, the front surface of the silicon wafer was subjected to secco etching to various depths, and three positions for measurement corresponding to the

supported positions Nos. 1 to 3 in the etched surface at each depth were observed by microscopic spectroscopy. With regard to a region in which pits formed from slip dislocations were not observed, the depth of the region from the front surface was measured.

2-3. Results and Discussion

In the case in which the heat treatment temperature was 1170°C or less, the depth of the region free of slip dislocations was 50 μm or more at all three positions for measurement. Therefore, it was assumed that occurrence of slip dislocations could be controlled throughout an entire in-plane direction and a region free of slip dislocations of sufficient depth could be obtained on the front surface side in the case in which the heat treatment temperature was 1170°C or less.

In contrast, in the case in which the heat treatment temperature was more than 1170°C, the depth of the region free of slip dislocations was about 10 μm or less at the position for measurement No. 1. Therefore, it was assumed that slip dislocations were inevitably created in a region of less than 20 μm from the front surface in the case in which the heat treatment temperature was more than 1170°C.

3. Summary

In the case in which vacancy heat treating is conducted under the conditions recited in claim 6 of the present invention, vacancies are formed in a way such as follows.

(1) a high concentration of vacancies are formed in the interior near the surface.

(2) vacancy concentration in the interior near the surface is higher than that in the mid-section. In particular, vacancy concentration in the mid-section of the silicon wafer is low.

Furthermore, a sufficient amount of vacancies are created even at a low temperature (1135 to 1170°C). Therefore, occurrence of slip dislocations can be controlled throughout an entire in-plane direction and a region free of slip dislocations having sufficient depth can be obtained.

Consequently, due to the subsequent SF nuclei heat treating, SF nuclei can be formed at high density in the interior near the surface, in which more gettering effect is required.

Also, since vacancy concentration in the mid-section of the wafer is low, high strength can be obtained in the mid-section (see description on page 14, lines 21 and 22). Furthermore, since vacancy heat treatment can be conducted at low temperature, the occurrence of slip dislocations can be prevented, and thereby, reduction of strength due to slip dislocation can be prevented. Therefore, sufficient strength as required for the entire silicon wafer can be obtained (see description on page 14, lines 21 and 22).

In contrast, in the first embodiment of Falster, the vacancy concentration near the surface is lower than that in the mid-section of the silicon wafer.

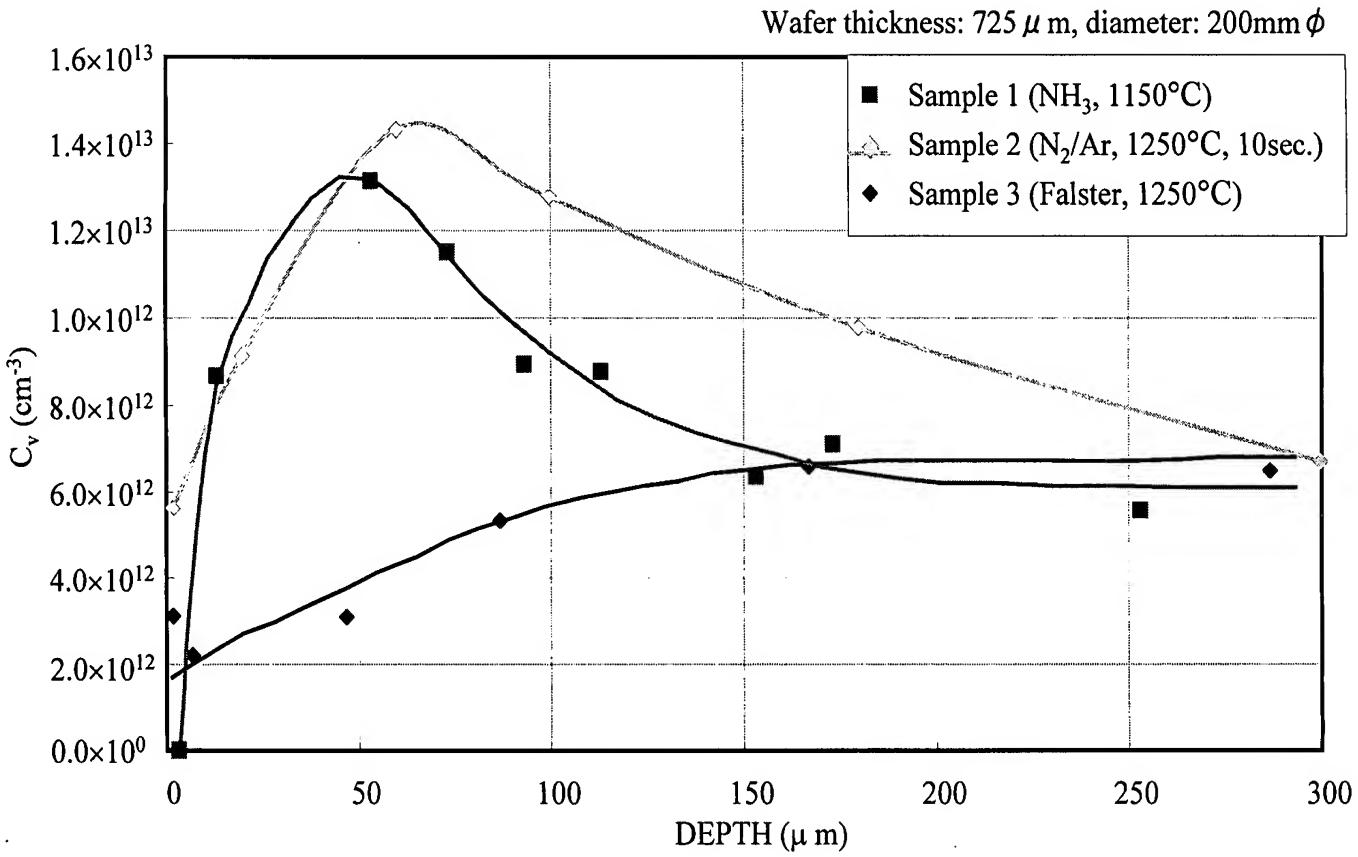
In Example 5 of Falster, slip dislocations are inevitably created in a region of less than 20 μm from the front surface.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

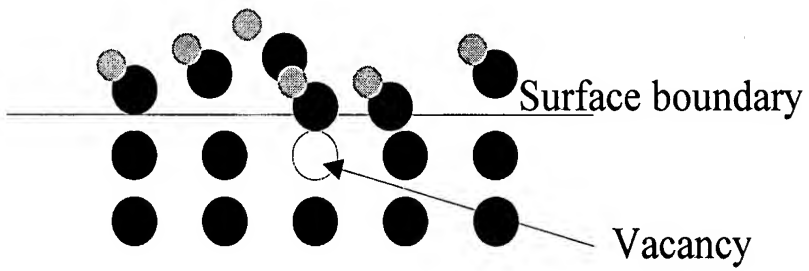
Date: 23 / Feb / 2006

Takaaki Shiota

T. Shiota

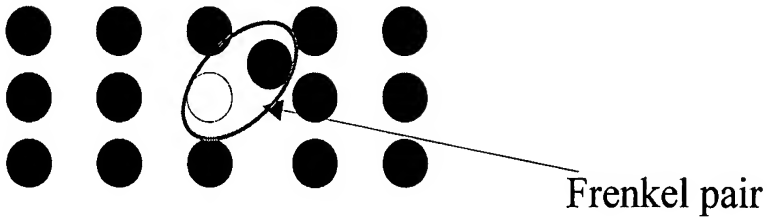


REFERNCE FIG. 1 EXPERIMENTAL DATA OF PROFILES OF FROZEN VACANCY CONCENTRATION



When surface of silicon wafer is nitrided, vacancies are formed and dispersed in a bulk portion.

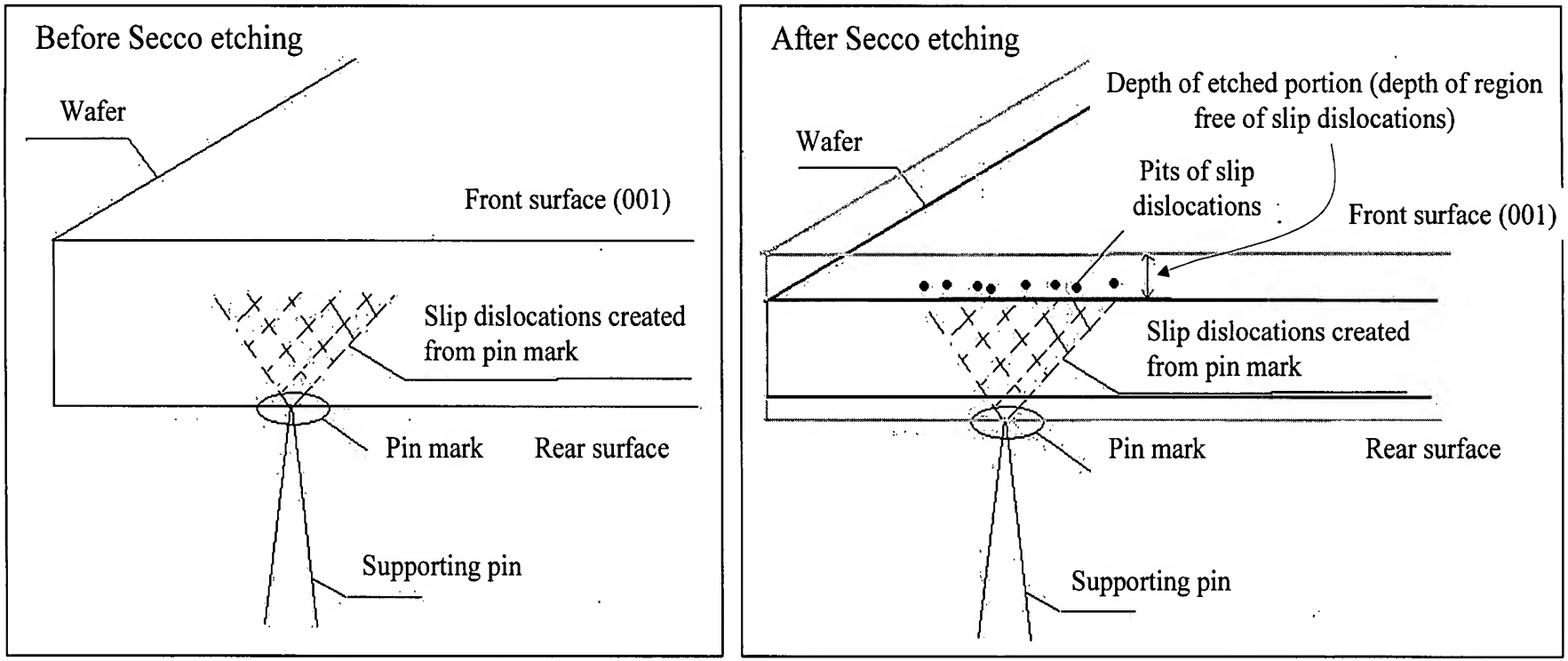
REFERENCE FIG. 2 (a) IMAGINARY VIEW OF VACANCY-INJECTION DUE TO SURFACE NITRIDING



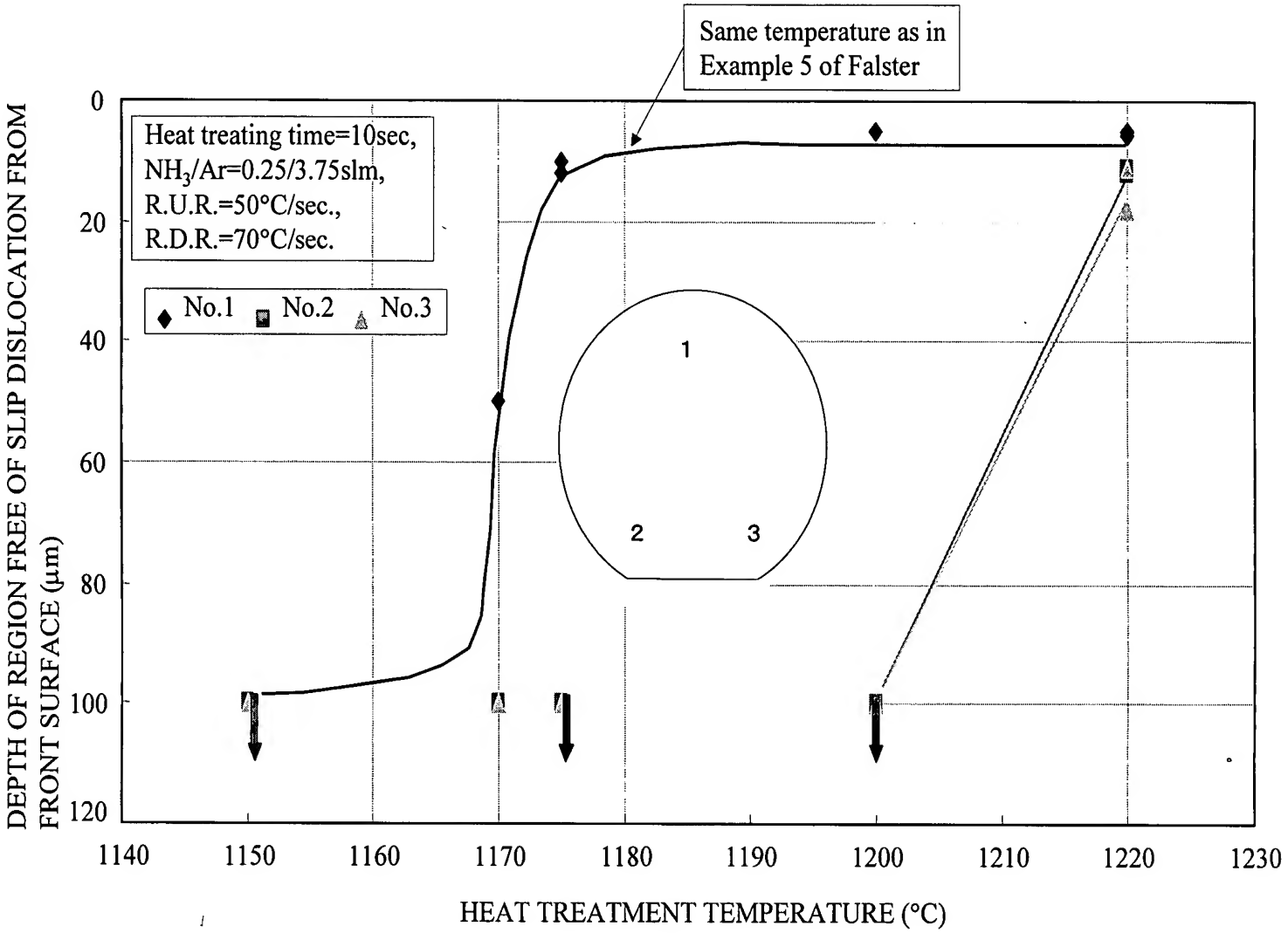
Vacancies/interstitial silicons are created.

Since interstitial silicon diffuses quickly, only vacancies are frozen after rapid cooling.

REFERENCE FIG. 2 (b) IMAGINARY VIEW OF VACANCY-FORMATION DUE TO CREATION OF FRENKEL PAIR

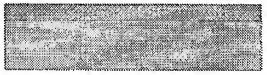
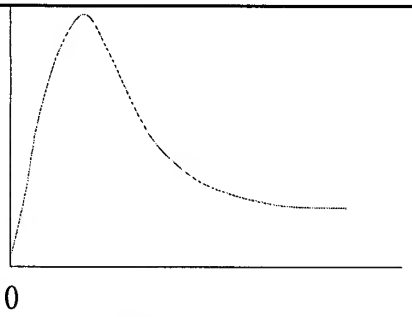
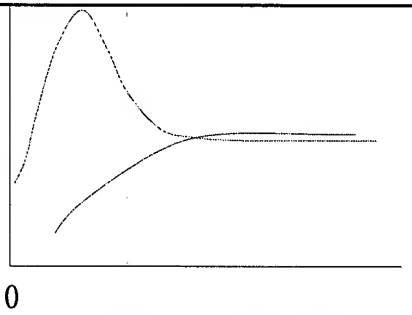
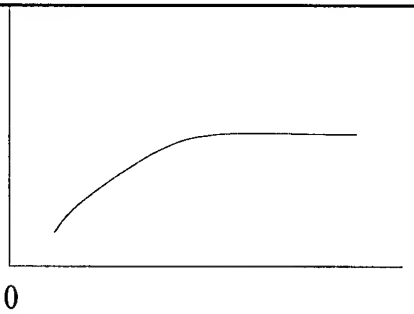


REFERENCE FIG. 3 SLIP DISLOCATIONS CREATED FROM SUPPORTED POSITIONS OF WAFER



REFERENCE FIG. 4 RELATIONSHIP BETWEEN DEPTH OF REGION FREE OF SLIP DISLOCATION AND HEAT TREATMENT TEMPERATURE IN ATMOSPHERE CONTAINING NH_3

REFERENCE TABLE 1 SUMMARY OF EXPERIMENTAL DATA

	Present invention	Vacancy heat treating in N_2	Citation (first embodiment of Falster)
Wafer subjected to vacancy heat treatment	No layer existing except native oxide layer in the surface 	No layer existing except native oxide layer in the surface 	Existing enhanced oxide layer in the surface 
Formation of vacancies	1. Surface nitriding using NH_3 (vacancies created (injected) from the surface) 2. Frenkel pairs not created.	1. Surface nitriding using N_2 (vacancies created (injected) from the surface) 2. Frenkel pairs also created.	1. Inert gas (N_2) (vacancies not created (injected) from the surface) 2. Frenkel pairs created.
Vacancy profile vertical scale: vacancy concentration horizontal scale: depth from wafer surface			
	(horizontal scale ranges from zero (surface) to half of wafer thickness)		
RTA tenperature	≦1170°C	=1250°C	=1250°C
Slip dislocations	can be controlled	present	present